Amendments to the Claims:

This listing of Claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-14 (Canceled).

15. (Previously presented) A method of operating a Dynamic Frequency Scaling (DFS) cache memory including a line buffer DFS cache memory and a DFS main cache memory associated therewith, the method comprising:

modifying access to the DFS cache memory based on whether the DFS cache memory is operating according to a low frequency DFS clock or a high frequency DFS clock, wherein modifying comprises:

accessing the DFS main cache memory without accessing the DFS line buffer cache memory when the DFS cache memory is operating according to the high frequency DFS clock; and

accessing the DFS line buffer cache memory responsive to a miss on accessing the DFS main cache memory when the DFS cache memory is operating according to the low frequency DFS clock.

16. (Original) A method according to Claim 15 wherein accessing the line buffer DFS cache memory further comprises:

accessing the DFS line buffer cache memory at a first time in a single low frequency DFS clock cycle of the low frequency DFS clock to determine whether data associated with an address is stored therein; and

accessing the DFS main cache memory at a second time in the single low frequency DFS clock cycle responsive to determining that the data is not stored in the DFS line buffer cache memory.

17. (Original) A method according to Claim 16 wherein accessing the DFS line buffer cache memory comprises beginning accessing the DFS line buffer cache memory during the first time in the single low frequency DFS clock cycle.

18. (Original) A method according to Claim 16 wherein the second time comprises a time interval in the single low frequency DFS clock cycle between completion of a single high frequency DFS clock cycle and completion of the single low frequency DFS clock cycle.

19. (Original) A method according to Claim 16 wherein the single low frequency DFS clock cycle comprises a time interval between two time adjacent low frequency DFS clock edges having no intervening low frequency DFS clock edges.

Claims 20-28 (Canceled).

29. (Original) A Dynamic Frequency Scaling (DFS) cache memory system comprising:

a line buffer cache memory configured to store line buffer cached tag and data information;

a line buffer cache memory enable circuit configured to enable access to the line buffer cache memory during an idle time in a single low frequency DFS clock cycle based on the DFS signal in an on state and configured to disable access to the line buffer cache memory based on the DFS signal in an off state;

a main cache memory configured to store main cached tag and data information; and

a main cache memory enable circuit configured to disable access to the main cache memory based on a DFS signal in the on state and configured to enable access to the main cache memory during the idle time based on the DFS signal in the on state and a miss on an access to the line buffer cache memory.

30. (Original) A DFS cache memory system according to Claim 29 wherein the main cache memory enable circuit is further configured to disable access to the main cache memory during the single low frequency DFS clock cycle prior to the idle time.

31. (Original) A Dynamic Frequency Scaling (DFS) cache memory system comprising:

a filter cache memory configured to store filter cached tag and data information;

a main cache memory configured to store main cached tag and data information; and

a main cache memory enable circuit configured to enable access to the main cache memory during an idle time in a single low frequency DFS clock cycle based on the DFS signal in the on state and a miss on the access to the filter cache memory and configured to disable access to the main cache memory during the idle time based on the DFS signal in the on state and a hit on the access to the filter cache memory.

32. (Original) A DFS cache memory system according to Claim 31 wherein the main DFS cache memory is configured to begin access during the idle time in the single low frequency DFS clock cycle.

33. (Original) A DFS cache memory system according to Claim 31 wherein the idle time comprises a time interval in the single low frequency DFS clock cycle between completion of a single high frequency DFS clock cycle and completion of the single low frequency DFS clock cycle.

34. (Original) A DFS cache memory system according to Claim 31 wherein the cache memory enable circuit further comprises:

a storage element circuit configured to store a result of the access to the filter cache memory on a transition of a DFS clock signal at a beginning of the idle time to provide a clocked filter cache hit/miss result; and

a multiplexer, coupled to the storage element, configured to select the clocked filter cache hit/miss result responsive to the DFS signal in the off state and configured to select the result of the access to the filter cache memory responsive to the DFS signal in the on state to provide a main cache memory enable/disable signal to the main cache memory.

35. (Original) A DFS cache memory system according to Claim 34 wherein the storage element circuit comprises a flip-flop circuit.

36. (Original) A DFS cache memory system according to Claim 31 wherein the DFS cache memory comprises a cache memory system configured to operate using a first clock signal having a first frequency in a first mode when the DFS signal is in the off state and configured to operate using a second clock signal have a second frequency that is less than the first frequency in a second mode when the DFS signal is in the on state.

37. (Original) A DFS cache memory system according to Claim 31 wherein the first mode comprises a high frequency mode and the second mode comprises a low frequency mode.